UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/762,572	01/23/2004	John Twynam	204552031600	3031

7590 06/12/2006

Barry E. Bretschneider
Morrison & Foerster LLP
Suite 300
1650 Tysons Boulevard
McLean, VA 22102

EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/762,572	TWYNAM, JOHN	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3 and 5-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/29/06 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, and 2 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. 5,192,987 in view of Yamashita et al. 6,995,397 B2. Khan discloses (see, for example, FIG. 5) a transistor (compound semiconductor FET) comprising a buffer layer (AlN layer) 38, substrate 37; a plurality of III-N layers comprising GaN layer 39 and $Al_xGa_{1-x}N$ layer 41; source contact (source electrode) 43, gate contact (gate electrode) 47, and drain contact (drain electrode) 44. Khan does not disclose an n-type delta doped GaN layer. However, Yamashita discloses (see, for example, FIG. 1) a semiconductor device comprising a channel layer 20 wherein the channel layer comprises an n-type undoped layer 22, and an n-type delta doped layer 21. In column 23, lines 1-6, Yamashita discloses that GaN may be used. In the abstract, Yamashita

discloses the electric field in the surface regions is weakened, thereby allowing the current drive force to increase. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an n-type delta doped GaN layer in order to increase the current drive force of the transistor.

Regarding the limitation "AlN layer" in line 2 of claim 1, see, for example, column 4, lines 19-20 wherein Khan discloses the buffer layer comprising aluminum nitride (AlN).

4. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yamashita et al. '397 B2 as applied to claims 1, and 2 above, and further in view of Phillips 6,770,902 B2. Khan in view of Yamashita does not disclose an insulating layer. However, Phillips discloses (see, for example, figure) a transistor comprising a gate insulation layer 32. In column 5, lines 58-65, Phillips discloses that the gate insulation layer forms a MISFET instead of a Schottky contact. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an insulating layer in order to form another semiconductor device such as a MISFET (instead of a Schottky contact).

5. Claims 5, and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yamashita et al. '397 B2 as applied to claims 1, and 2 above, and further in view of Inoue 6,639,255 B2. Khan in view of Yamashita does not disclose each of the semiconductor layers being of a C-plane Ga-surface type. However, Inoue discloses (see, for example, abstract) a semiconductor device comprising layers that have c facets of Ga atoms (C-plane Ga-surface type). In column 10, lines 65-67, Inoue discloses that such a structure prevents

an increase of the source resistance and reduction of the leakage current. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have each of the semiconductor layers being of a C-plane Ga-surface type in order to prevent an increase of the source resistance and reduce the leakage current.

Regarding lines 5-6 of claim 5, Khan in view of Yamashita does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of $1X10^{13}$ cm^{-2} to $2 X 10^{13}$ cm^{-2}." However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to increase the current drive force by weakening the electric field in the surface region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-N layer is within a range of $1X10^{13}$ cm^{-2} to $2 X 10^{13}$ cm^{-2} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to increase the current drive force by weakening the electric field in the surface region. See In re Aller, 105 USPQ 233.

Regarding lines 5-6 of claim 6, Khan in view of Yamashita does not disclose the sheet doping concentration of the n-type delta doped III-N layer being within a range of $5X10^{12}$ cm^{-2} to $1.5 X 10^{13}$ cm^{-2}." However, it was well within the skills of an artisan in the art to optimize the performance of a semiconductor device by adjusting the sheet doping concentration of a n-type delta doped III-N layer in order to increase the current drive force by weakening the electric field in the surface region. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention was made to have sheet doping concentration of the n-type delta doped III-

N layer is within a range of $5X10^{12}$ cm^{-2} to $1.5 X 10^{13}$ cm^{-2} because it was well within the skills of an artisan to optimize the performance of a semiconductor device by adjusting the sheet doping concentration in order to increase the current drive force by weakening the electric field in the surface region. See In re Aller, 105 USPQ 233.

Regarding the limitation "substrate is sapphire" in line 2 of claim 5, see, for example, column 2, lines 41-43, wherein Khan discloses the material of the substrate being sapphire.

Regarding the limitation "substrate is SiC" in line 2 of claim 6, see, for example, column 6, lines 7-10, wherein Khan discloses the material of the substrate being silicon carbide (SiC).

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Khan et al. '987 in view of Yamashita et al. '397 B2 as applied to claims 1, and 2 above, and further in view of Abrokwah et al. 5,895,929. Khan in view of Yamashita does not disclose an electronic circuit provided with the compound semiconductor FET. However, Abrokwah discloses (see, for example, column 1, lines 15-46) FETS being part of electronic circuits such as logic and control circuits, high speed digital circuits, and the like. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to have an electronic circuit provided with the compound semiconductor FET in order to integrate the transistors in more robust devices.

Response to Arguments

6. Applicant's arguments with respect to claims 1-3, and 5-7 have been considered but are moot in view of the new ground(s) of rejection.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Eugene Lee
June 5, 2006

EUGENE LEE
PRIMARY EXAMINER